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UTILITY PATENT APPLICATION TRANSMITTAL LETTER

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. 149733/97

To the Assistant Commissioner for Patents:

Transmitted herewith for filing is the patent application of:
Yoshiaki YAMAMOTO
corresponding to Japanese application No. 149733/1997, filed June 6, 1997,
entitled: METHOD OF FABRICATING SEMICONDUCTOR DEVICE FOR PREVENTING RISING-UP OF SILISIDE

Enclosed are:

X	16 pages of specification.
X	nine sheets of formal drawings.
X	a newly-executed declaration of the inventor.
	a copy of an executed declaration of the inventor from prior application Serial No. , filed .
	incorporation by reference. The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied as indicated in the preceding box, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
X	an assignment of the invention to NEC Corporation, including assignment cover sheet.
X	Information Disclosure Statement with Form PTO-1449.
X	copies of the Information Disclosure Statement citations.
	preliminary amendment.
X	return receipt postcard (MPEP 503), specifically itemized.
	a verified statement to establish small entity status under 37 CFR 1.9 and 1.27.
	a verified statement to establish small entity status filed in prior application. Status is still proper and desired.
X	a certified copy of the Japanese Priority Document.
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If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information.*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP)

of prior application No. , filed .

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(Y&T 12/97)

UTILITY PATENT APPLICATION TRANSMITTAL LETTER (continued)	Docket No. 149733/97

CLAIMS AS FILED

	NO. FILED	NO. EXTRA	RATE	FEE
BASIC FEE			$ 790	$ 790
TOTAL CLAIMS	20 - 20 =	0	x$ 22	0
INDEPENDENT CLAIMS	2 - 3 =	0	x$ 82	0
MULTIPLE DEPENDENT CLAIM PRESENT			$ 270	
			TOTAL	$ 790
If applicant has small entity status under 37 CFR 1.9 and 1.27, then divide total fee by 2, and enter amount here.			**SMALL ENTITY TOTAL**	$

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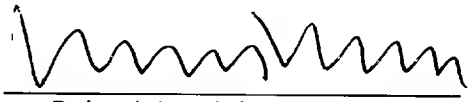

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June 3, 1998

METHOD OF FABRICATING SEMICONDUCTOR DEVICE FOR PREVENTING RISING-UP OF SILISIDE

Background of the Invention

1. Field of the Invention

The present invention relates to a method fablicating a semiconductor device, more particularly to a method fabricating a semiconductor device for preventing rising-up of siliside.

A high integration of semiconductor integrated circuits such as LSIs has developed micronizing of devices. For example, impurity diffusion layers in a source and drain regions are formed to be shallow and areas of them are made small. Moreover, a width of a wirings connecting the devices are also narrowed. For this reason, electric resistances of the diffusion layers and the wirings are increased, so that a high speed operation of the devices is obstructed. From such circumstances, in the recent semiconductor devices, the attempt is made to form the surface of the impurity diffusion layer by high melting point metal silicides, particularly by titanium silicide, whereby a high speed operation of the devices can be achieved by an increase in the resistance of the impurity diffusion layer.

For the formation of the titanium silicide layer, United States Patent No. 4,855,798 discloses the formation of the titanium silcide layer using a self-alignment manner. The method to form the titanium silicide layer in

the self-alignment manner will be described with reference to Figs. 3(a) to 3(g).

As shown in Fig. 3(a), the field oxide film 2, the gate oxide film 3, the gate electrode 4 and the side wall film 5 are formed on the semiconductor substrate 1. The exposed portions 6 of the semiconductor substrate 1 act as a diffusion layer region after impurity ions are injected thereto.

Next, a protection oxide film 7 for the ion injection is formed on the entire surface of the resultant structure using a CVD method, for example, thereby forming the diffusion layer 9 (Fig. 3(b)). Subsequently, a thermal treatment at a temperature of not less than 900 ℃ is performed to activate the diffusion layer 9. That is, the activated diffusion layer 14 is formed.

Thereafter, the protection oxide film 7 is removed, and further a natural oxide film is removed prior to a Ti sputtering (Fig. 3(c)).

Next, as shown in Fig. 3(d), the titanium film 11 is grown on the entire surface of the resultant structure by a sputtering method, for example. The titanium silicide film 11 is subjected to a thermal treatment under the conditions that a temperature is not more than 700 ℃ at an inertia gas atmosphere, for example, a nitrogen atmosphere. Thus, the titanium silicide layer 12 of C49 phase formed of high resistance $TiSi_2$ is formed (a first sinter). At this time, the titanium silicide layer 12 is formed only on

the gate electrode 4 and the diffusion layer 9 in a self-aligned manner Fig. 3(e).

Subsequently, the non-reacted titanium film 11 on the field oxide film 2 and the side wall film 5 is removed (Fig. 3(f)). Furthermore, a thermal treatment at a temperature of not less than 800 ℃ is performed. As a result of the thermal treatment, the titanium silicide film of C54 phase formed of low resistance $TiSi_2$ as shown in Fig. 3(g) is formed (a second sinter).

However, when the titanium silicide films are formed by the foregoing method, the development of micronizing of the devices has created the problems of an electrical short-circuit between the gate electrode and the diffusion layers acting as the source/drain regions and between the diffusion layers adjacent to each other. The electrical short-circuits inherently originate from rising-up of the titanium silicide onto the region where the titanium silicide is not formed, that is, onto the side wall film for separating the gate electrode and the diffusion layers and onto the field oxide film for separating the diffusion layers. Hereinafter, such phenomenon is referred to as "a rising-up" . Alternately, the electrical short-circuits originate from the formation of the conductive material. In order to prevent the rising-up of the titanium silicide and the formation of the conductive material, lengthening of an etching time to etch the non-reactive titanium silicide causes the titanium

silicide on the diffusion layer to be etched excessively, leading to an abuse that the diffusion layer resistance increases.

From such viewpoint, several methods to prevent the rising-up due to the expansion of the titanium silicide into the region except that where the titanium silicide is to be formed have been proposed.

One of them is disclosed in Japanese Patent Laid Open No. Sho 61-150216. In this method, a titanium film is formed on a silicon substrate. Thereafter, the first sinter is performed at a comparatively low temperature of 400 to 600 ℃, whereby the titanium film is converted to a titanium silicide film by so-called siliciding reaction. A non-reactive titanium film is removed, thereby forming a high resistance titanium silicide film on diffusion layers and a gate electrode. Thereafter, the second sinter is performed at a temperature not less than 800 ℃, thereby converting the high resistance titanium silicide film to a low resistance titanium silicide film. Because the first sinter is performed at the comparatively low temperature of 400 to 600 ℃, this method has a feature in that the rising-up of the titanium silicide film can be prevented.

Another method is disclosed in Japanese Patent Laid Open No. Sho 59-126672. The structure of the semiconductor device manufactured by this method is shown in Fig. 4. In this method, in order to suppress the rising-up of the titanium silicide film on the side wall film and the

reaction of the titanium film with the side wall film, the side wall film is formed of the SiN film which is not prone to react with the titanium film.

However, the above-described methods have posed the following new problems.

The firstly described method involves the problem that with the micronizing of the diffusion layers and the gate electrode, a desired resistance can not be obtained. The reason is that because the first sinter temperature is low, the resistance of the titanium silicide is high, and the layer resistance of the diffusion layer after the second sinter is not below a desired value. In order to obtain the diffusion layer resistance below the desired value, if the second sinter temperature is increased, the problem that the titanium silicide is condensed occurs. For this reason, under the low first sinter temperature, the low resistance of the diffusion layer can not be achieved in spite that the rising-up of the titanium silicide can be suppressed.

In the secondly described method, though the electrical short-circuit between the gate electrode and the diffusion layer can be suppressed, it is impossible to suppress the electrical short-circuit between the diffusion layers adjacent to each other.

As described above, the electrical short-circuits between the gate electrode and the diffusion layer and between the diffusion layers adjacent to each other can not

be necessarily perfectly suppressed with the conventional technologies.

In order to suppress such the electrical short-circuit perfectly, factors of the rising-up of the titanium silicide were investigated. The rising-up of the Ti silicide is more significant in the P-type diffusion layer, so that an attention was paid on P-type ion injection species. Fig. 5 shows a state where the rising-up of the Ti silicide occurs in the case where BF^{2+} (mass: 49) and B^{+} (mass: 11) are used as the ion injection species. For the P-type diffusion layer to which BF^{2+} (mass:49) is injected, the rising-up of the Ti silicide is shown. On the contrary, for the P-type diffusion layer to which B^{+} (mass:11), no rising-up is shown. From this fact, it was proved that F in the BF^{2+} (mass: 49) that is the P-type ion injection species is allowed to be remained in the field oxide film and the side wall film, and a Ti silicide reaction inductively occurs on the field oxide film and the side wall film during performing the Ti silicide reaction, thereby creating the rising-up of the Ti silicide.

If the P-type diffusion layer is formed using B^{+} (mass: 11) as the ion injection species, the rising-up of the Ti silicide can be suppressed. However, it is impossible to form shallow diffusion layers, so that micronizing of the semiconductor integrated circuit can not be achieved with the use of B^{+} (mass:11) as the ion

injection species.

Summary of the Invention

From viewpoint of the above described circumferences, the object of the present invention is to provide a formation method of a Ti silicide applied to manufactures of the semiconductor devices, more particularly to a method for forming good quality products stably without producing defective products due to an electrical short-circuit between a gate electrode and a diffusion layer and between diffusion layers adjacent to each other.

The method of the present invention was proposed in order to achieve the above-described object.

A method of fabricating a semiconductor device comprising, forming an isolation region around a predetermined area of a semiconductor substrate, selectively forming an insulating layer on said predetermined area, selectively forming an electrode on said insulating layer, injecting an impurity ion in said substrate which is between said electrode and said isolation region, applying heat of a first temperature to said substrate, and applying heat of a second temperature higher than said first temperature to said substrate for activating said impurity ion after applying heat of said first temperature.

The method of the present invention is featured by that a low temperature thermal treatment is carried out

between the ion injection for forming the diffusion layer and the activation of the diffusion layer, thereby discharging fluorine produced from the ion injection species to the outside from a surface of the insulating film, a surface of the side wall, the silicon semiconductor substrate, and an interface between the semiconductor substrate and the isolation region. The low temperature thermal treatment is preferably carried out subsequent to the activation step consecutively in the same apparatus.

An operation of the present invention will be described with an example using an ion injection species which includes fluorine.

The method of the present invention has an feature that the step for removing fluorine injected into the surface of the field oxide film, the surface of the side wall film, the semiconductor substrate, the interface between the semiconductor substrate and the field oxide film. The reason why fluorine is removed as follows. Because of the formation of the P-type diffusion layer, fluorine injected into the field oxide film, the side wall film and the semiconductor substrate induces during the first sinter of the Ti silicide formation step, the rising-up of the Ti silicide on the portions of the field oxide film and side wall film where the Ti silicide should not be formed. When the rising-up of the Ti silicide occurs, the electrical short-circuits between the gate electrode and the diffusion layer and between the diffusion layers

adjacent to each other are caused. Therefore, the method of a semiconductor device is intended to suppress the rising-up of the Ti silicide by removing fluorine.

In order to remove fluorine, the low temperature thermal treatment is carried out prior to the step for activating the diffusion layer. Removing the fluorine enables to stably obtain good quality products free from the rising-up of the Ti silicide, without producing defective products due to an electrical short-circuit.

Brief Description of the Drawings

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, in which;

Figs. 1(a) to 1(h) are a schematic section view showing a first application example of a Ti silicide formation method of first and second embodiments, according to a sequence of steps thereof;

Fig. 2 shows a temperature profile when a low temperature thermal treatment and an activation thermal treatment are simultaneously performed in the second embodiment of the present invention;

Figs.3(a) to 3(g) are a schematic section view showing a sequence of steps of an example of a conventional Ti silicide formation method;

Fig. 4 is an example of a section structure after the formation of the Ti silicide in the conventional

technology;

Figs. 5(a) and 5(b) are a SEM photograph of the semiconductor device which has the configuration shown in Fig. 4, when viewed from an obliquely above direction, specifically, Figs. 5(a) and 5(b) show a micro-pattern formed on a semiconductor substrate, which shows a state of a rising-up of a Ti silicide, show that the degree of the rising-up differs depending on an injection species injected, and Fig. 5(a) shows the case where B^+(mass:11) is used and Fig. 5(b) shows the case where BF^{2+}(mass:49) is used.

Fig. 6 is a graph showing a depth profile of concentrations of boron and fluorine in BF^{2+}(mass:49)that is a P-type ion injection species; and

Fig. 7 shows a relation between a yield ratio and the fluorine concentration obtained when the first embodiment is performed.

Detailed Description of the Preferred Embodiments

Embodiments of the present invention will be described with reference to the accompanying drawings below in detail.

(Embodiment 1)

This embodiment applies the first invention, and this embodiment will be described with reference to Figs. 1(a) to 1(h).

As shown in Fig. 1(a), the field oxide film 2, the gate oxide film 3, the gate electrode 4 and the side wall

film 5 are formed on the silicon substrate 1. Impurity ions are injected into the exposed portions of the silicon substrate 6, and these portions act as a diffusion layer region, respectively.

Subsequently, a protection oxide film 7 for an ion injection is formed on the entire surface of the resultant structure using a CVD method. Thereafter, the impurity ions 8 are injected, thereby forming the diffusion layer 9 (Fig. 1(b)). Here, the description is made for formation of a P-type diffusion layer. As P-type impurities, BF^{2+} (mass: 49) ions capable of forming a shallow junction are injected into the entire surface of the resultant structure of Fig. 1(a), under the conditions that an acceleration voltage is 30 KeV and an impurity concentration is 3E15 cm^{-2}. At this time, the depth profile of concentrations of boron and fluorine that are component elements of the ion injection species is determined depending on injection energy, in which B exhibits the maximum concentration near at about 30 nm and F exhibits it near at about 25 nm, as shown in Fig. 8.

Next, a thermal treatment is performed at a nitrogen gas atmosphere using a diffusion furnace, under the conditions that a temperature is 700 ℃ and a treatment time is 60 minutes (Fig. 1(c)). During the thermal treatment, F (fluorine) 10 existing in the field oxide film 2, the side wall film 5, the silicon substrate 9 and the interface between silicon substrate 1 and the field

oxide film 2 are discharged as an out gas. Hence, the F concentrations in the field oxide film 2, the side wall film 5, the silicon substrate 1 and the interface between the silicon substrate 9 and the field oxide film 2 become 1E20 atom/cm^3 or less.

Subsequently, a thermal treatment at a temperature of 1000 ℃ and for 10 seconds is performed using a lamp annealing apparatus, thereby activating the diffusion layer. That is, the activated diffusion layer 14 is formed. Here, if a low temperature thermal treatment is performed after the activation of the diffusion layer 14, F will combine with Si and the like, disenabling an annealing-out of the fluorine. Therefore, the low temperature thermal treatment should be effectively performed prior to the thermal treatment for activating the diffusion layer.

Thereafter, the protection oxide film 7 is removed using a RIE etching apparatus and natural oxide films formed on the diffusion layer and the gate electrode are removed using 1 : 100 DHF liquid, prior to a Ti sputtering (Fig. 1(d)).

Next, as shown in Fig. 1(e), the Ti film 11 is formed to a thickness of 30 nm on the entire surface of the resultant structure by sputtering. A thermal treatment at a temperature of 700 ℃ and for 30 seconds is performed using a lamp annealing apparatus, thereby forming the Ti silicide layer 12 of C49 phase formed of high resistance

$TiSi_2$ (a first sinter) (Fig. 1(f)). At this time, the Ti silicide layer 12 is formed only on the gate electrode 3 and the diffusion layer 9 in a self-aligned manner.

Then, the non-reactive portions of the Ti film 11 on the field oxide film 2 and the side wall film 5 are removed using an aqueous per-ammonium solution (Fig. 1(g)).

Thereafter, a thermal treatment at a temperature of 850 ℃ for 10 seconds is further performed using a lamp annealing apparatus. As a result, the Ti silicide layer 13 of C54 phase formed of a low resistance $TiSi_2$ as shown in Fig. 1(h) is formed (a second sinter).

The Ti silicide film 13 formed as described above exhibits no rising-up onto the field oxide film 2 and the side wall 5. The low sheet resistivity of the Ti silicide film of 10 Ω/□ or less can be obtained, so that an increase in an operation speed of the devices can be achieved and the yield ratio of the good quality products increases as shown in Fig. 7.

(Embodiment 2)

This embodiment applies to the second invention of this application. This embodiment will be described with reference to Figs. 1(a) to 1(h).

First, as shown in Fig. 1(a), similar to the first embodiment, the field oxide film 2, the gate oxide film 3, the gate electrode 4 and the side wall film 5 are formed on the silicon substrate 1. Impurity ions are injected into

the exposed portions of the silicon substrate 6, and these portions act as a diffusion layer region, respectively.

Subsequently, a protection oxide film 7 for an ion injection is formed on the entire surface of the resultant structure using a CVD method. Thereafter, the impurity ions 8 are injected, thereby forming the diffusion layer 9 (Fig. 1(b)). Here, similar to the first embodiment, the description is made for formation of a P-type diffusion layer. As P-type impurities, BF^{2+} (mass: 49) ions capable of forming a shallow junction are injected into the entire surface of the resultant structure of Fig. 1(a), under the conditions that an acceleration voltage is 30 KeV and an impurity concentration is 3E15 cm^{-2}. At this time, the depth profile of concentrations of boron and fluorine that are component elements of the ion injection species is determined depending on injection energy, in which B exhibits the maximum concentration near at about 30 nm and F exhibits it near at about 25 nm, as shown in Fig. 6.

Subsequently, a thermal treatment at a temperature of 1000 ℃ for 10 seconds is performed for activating the impurity ions using a lamp annealing apparatus. As shown in Fig. 2, a temperature is changed. In the step a of Fig. 2, fluorine is discharged as out-gas from the field oxide film 2, the side wall film 5, the silicon substrate 1 and the interface between the silicon substrate 1 and the field oxide film 2 (Fig. 1(c)). Hence, the F concentrations in the field oxide film 2, the side wall film 5, the silicon

substrate 1 and the interface between the silicon substrate 1 and the field oxide film 2 become 1E20 atom/cm^3 or less. In the step b of Fig. 2, the activation of the impurity ions is performed. That is, the activated diffusion layer 14 is formed. Thus, it is unnecessary to increase the number of the steps and manufacturing apparatuses.

Next, the protection oxide film 7 is removed using a RIE etching apparatus (Fig. 1(d)). Thereafter, natural oxide films formed on the diffusion layer and the gate electrode are removed using 1 : 100 DHF liquid, prior to a Ti sputtering.

Subsequently, as shown in Fig. 1(e), the Ti film 11 is formed to a thickness of 30 nm on the entire surface of the resultant structure by sputtering. A thermal treatment at a temperature of 700 ℃ for 30 seconds is performed using a lamp annealing apparatus, thereby forming the Ti silicide layer 12 of C49 phase formed of high resistance $TiSi_2$ (a first sinter) (Fig. 1(f)). At this time, the Ti silicide layer 12 is formed only on the gate electrode 3 and the diffusion layer 9 in a self-aligned manner.

Then, the non-reactive portions of the Ti film 11 on the field oxide film 2 and the side wall film 5 are removed using an ammonium hydroxide peeroxide mixture (Fig. 1(g)).

Thereafter, a thermal treatment at a temperature of 850 ℃ for 10 seconds is further performed using a lamp annealing apparatus. As a result, the Ti silicide layer 13

of C54 phase formed of low resistance $TiSi_2$ as shown in Fig. 1(h) is formed (a second sinter).

The Ti silicide film 13 formed as described above exhibits no rising-up onto the field oxide film 2 and the side wall 5. The low sheet resistivity of the Ti silicide film of 10 Ω/□ or less can be obtained, so that an increase in an operation speed of the devices can be achieved.

The Ti silicide formed using the present invention reduces the fluorine concentrations in the field oxide film and the side wall oxide film, whereby the rising-up of the Ti silicide can be suppressed and good quality products can be stably obtained without electrical short-circuits between the gate electrode and the diffusion layer as well as between the diffusion layers adjacent to each other.

Although the preferred embodiments of the present invention have been described in detail, it should be understood that various changes, substitutions and alternations can be made therein without departing from spirit and scope of the inventions as defined by the appended claims.

What is claimed is:

1. A method fabricating a semiconductor device comprising:

forming a field oxide film on a semiconductor substrate to form an element isolation region;

forming a side wall film formed of an insulation material on a side wall of a gate electrode which is formed on said semiconductor substrate;

injecting ion injection species into said semiconductor substrate using said gate electrode as a mask, thereby forming a diffusion layer;

activating said diffusion layer by a first thermal treatment;

depositing titanium on the entire surface of said semiconductor substrate and performing a second thermal treatment, thereby forming a Ti silicide either on said gate electrode or on said diffusion layer in a self-aligned manner; and

partially removing the titanium which is not converted to the Ti silicide,

wherein a third thermal treatment at a temperature lower than that of the first thermal treatment for the activation is carried out between the ion injection for forming said diffusion layer and the first thermal treatment for activating said diffusion layer, thereby discharging fluorine produced from the ion injection species to the outside from a surface of said field oxide film, a surface of said side wall film, said semiconductor

substrate, and an interface between said semiconductor substrate and said field oxide film.

2. The method as claimed in claim 1, wherein said third thermal treatment is consecutively performed in the same apparatus as that of said first thermal treatment for activating said diffusion layer.

3. The method as claimed in claim 1, wherein said ion injection species injected into said diffusion layer are ions including fluorine and boron.

4. The method as claimed in claim 1, wherein a fluorine concentration is set to be 1E20 atom/cm^3 or less by said third thermal treatment.

5. The method as claimed in claim 1, wherein a temperature of said third thermal treatment is at a range of 300 to 750 ℃.

6. The method as claimed in claim 1, wherein an apparatus for carrying out said third thermal treatment is a diffusion furnace, a RTP apparatus and a hot plate.

7. A method of fabricating a semiconductor device comprising:

forming an isolation region around a predetermined area of a semiconductor substrate;

selectively forming an insulating layer on said predetermined area;

selectively forming an electrode on said insulating layer;

injecting an impurity ion in said substrate which

is between said electrode and said isolation region;

applying heat of a first temperature to said substrate; and

applying heat of a second temperature higher than said first temperature to said substrate for activating said impurity ion after applying heat of said first temperature.

8. The method as claimed in claim 7, wherein said impurity ion includes fluorine.

9. The method as claimed in claim 8, wherein said applying heat of said first temperature applies said semiconductor device to discharge fluorine included in said isolation region.

10. The method as claimed in claim 7, further comprises selectively forming a siliside on said electrode.

11. The method as claimed in claim 10, wherein said siliside has C49 phase.

12. The method as claimed in claim 11, further comprises changing a phase of said siliside from C49 to C54.

13. The method as claimed in claim 12, wherein said impurity ion includes fluorine.

14. The method as claimed in claim 13, wherein said applying heat of said first temperature applies said semiconductor device to discharge fluorine included in said isolation region.

15. The method as claimed in claim 7, further comprises forming a side wall to a side of said electrode.

16. The method as claimed in claim 15, further comprises selectively forming a siliside on said electrode.

17. The method as claimed in claim 16, wherein said siliside has C49 phase.

18. The method as claimed in claim 17, further comprises changing a phase of said siliside from C49 to C54.

19. The method as claimed in claim 15, wherein said impurity ion includes fluorine.

20. The method as claimed in claim 19, wherein said applying heat of said first temperature applies said semiconductor device to discharge fluorine included in said isolation region and said side wall.

Abstract of the Disclosure

Disclosed is a manufacturing method of a semiconductor device which comprises which comprises an element isolation region formation step; a side wall formation step; a diffusion layer formation step; an activation step; a silicide formation step; and a removing step. The element isolation region formation step is the one for forming a field oxide film on a semiconductor substrate to form an element isolation region. In order to form a diffusion layer by introducing impurities into the semiconductor substrate, after injecting the fluorides (ion injection species) of elements into the semiconductor substrate, a thermal treatment is performed at a lower temperature than that of a thermal treatment for activating the diffusion layer prior to the activation of the diffusion layer, and fluorine produced from the ion injection species is discharged to the outside.

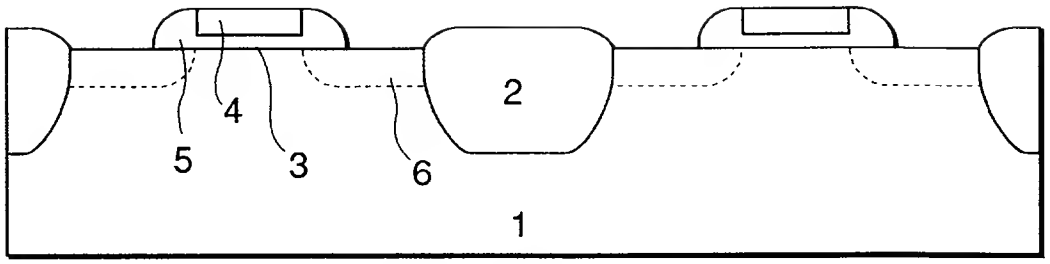


Fig.1(a)

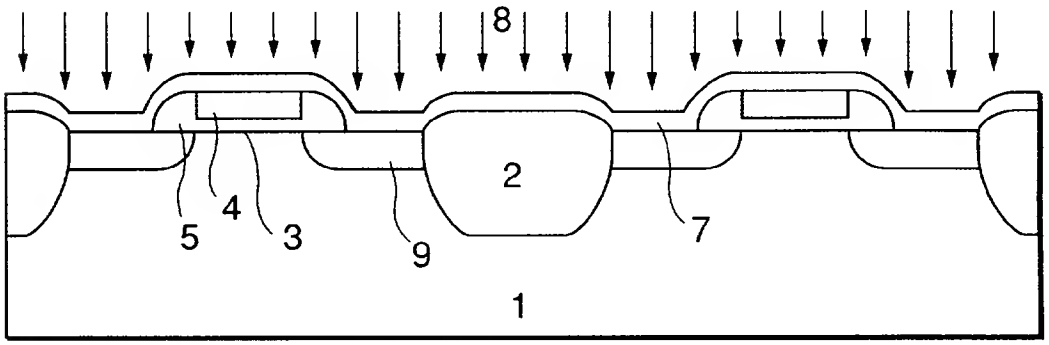


Fig.1(b)

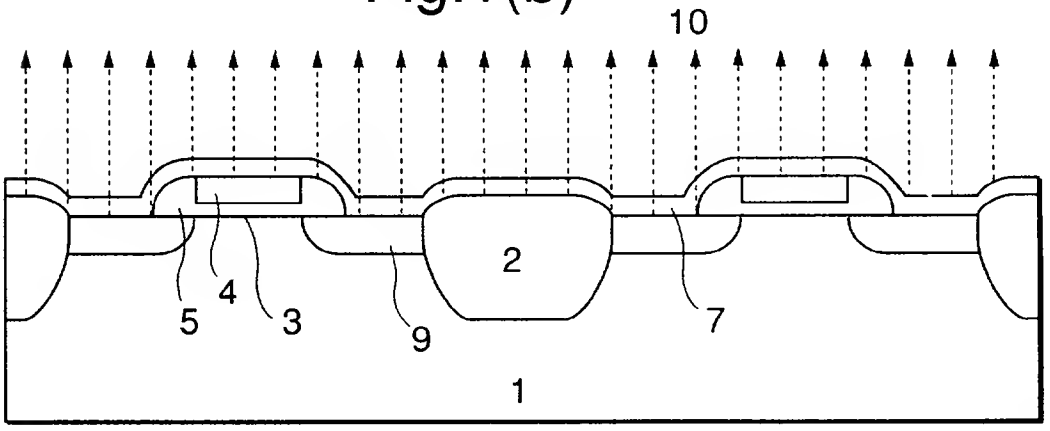


Fig.1(c)

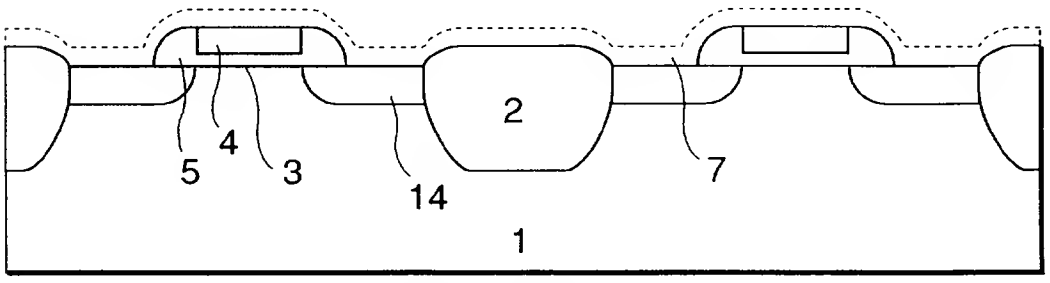


Fig.1(d)

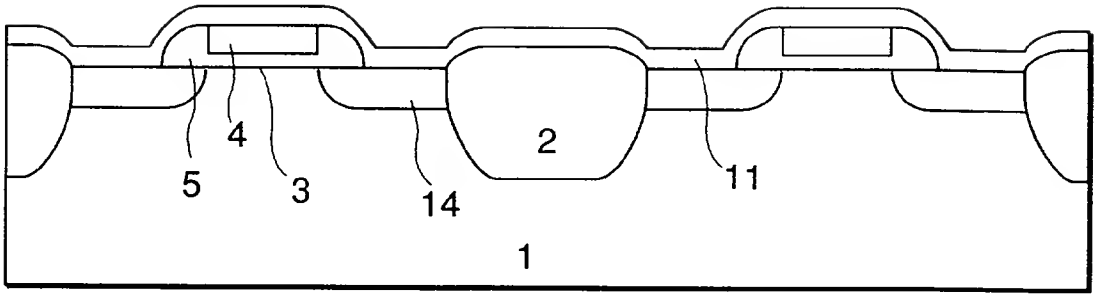


Fig.1(e)

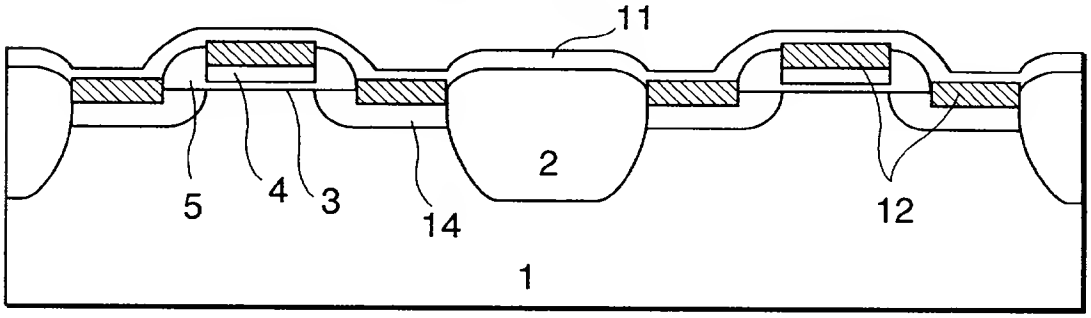


Fig.1(f)

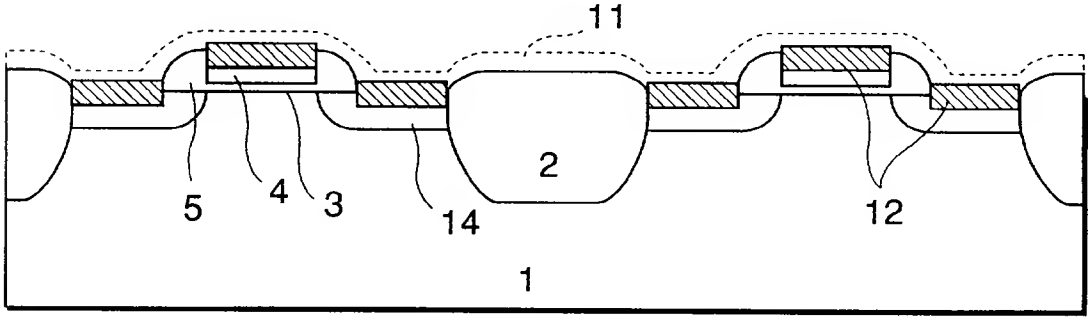


Fig.1(g)

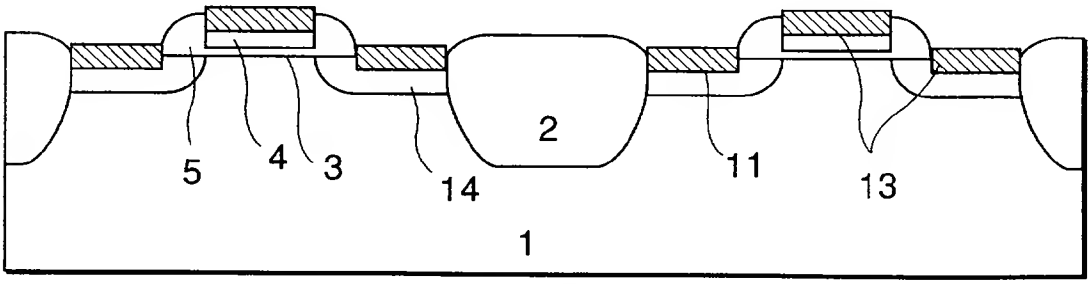
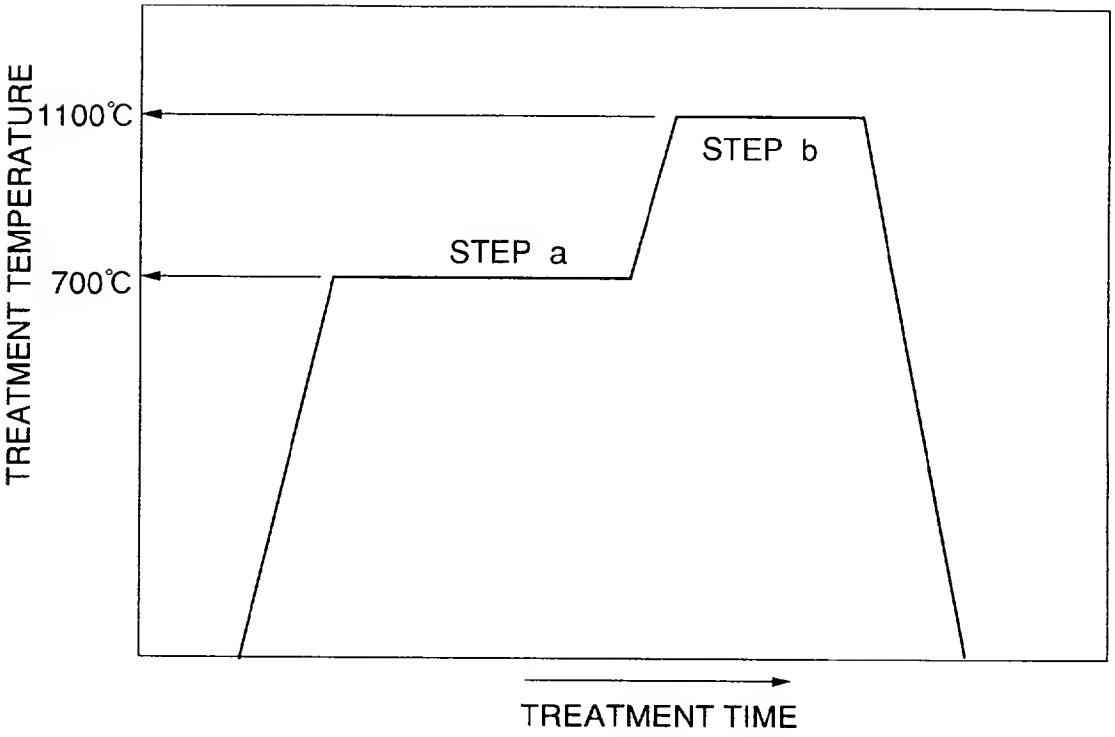


Fig.1(h)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TREATMENT TIME

Fig.2

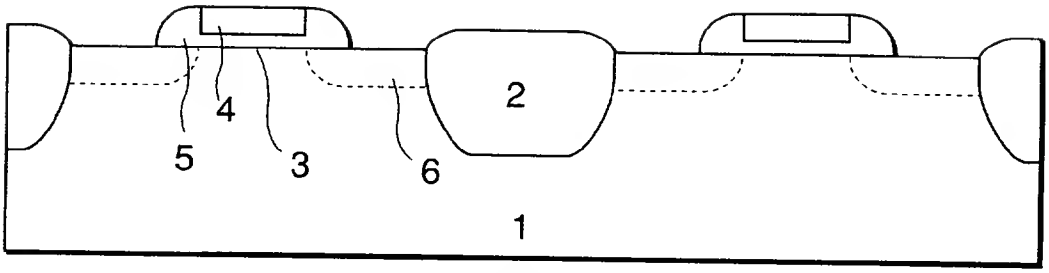


Fig.3(a)

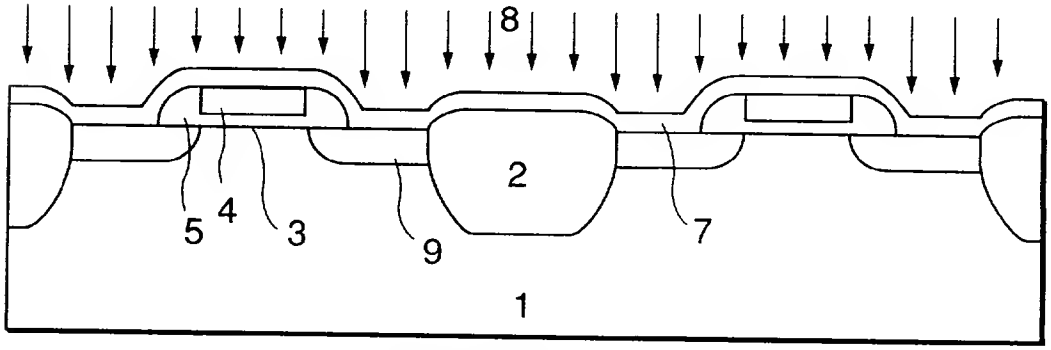


Fig.3(b)

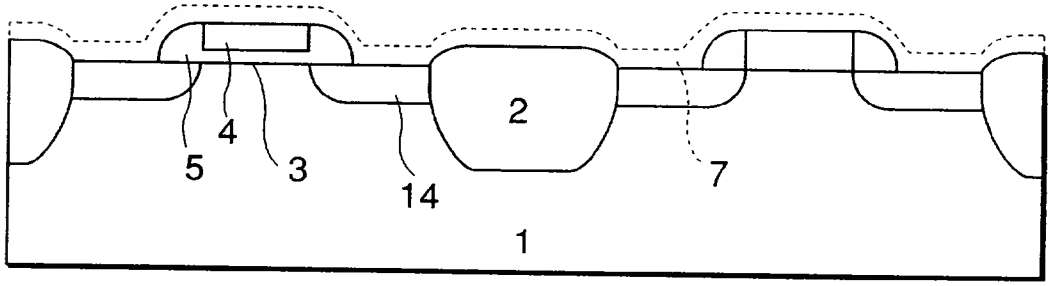


Fig.3(c)

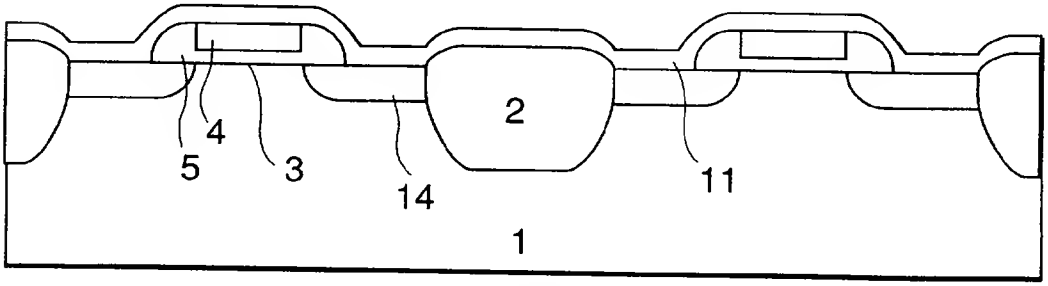


Fig.3(d)

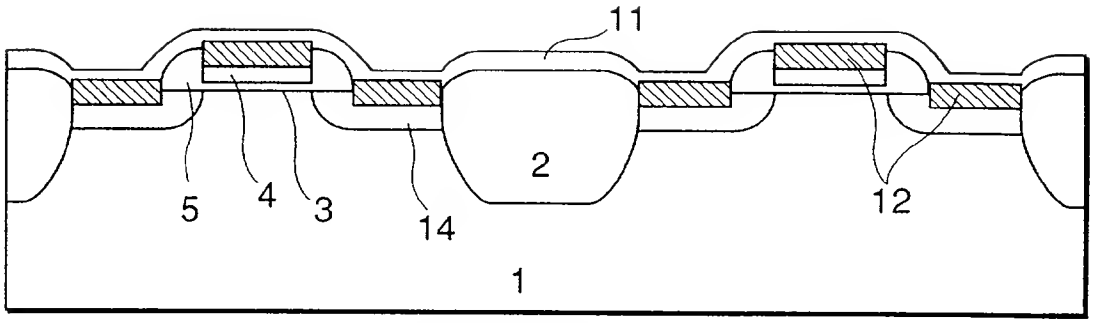


Fig.3(e)

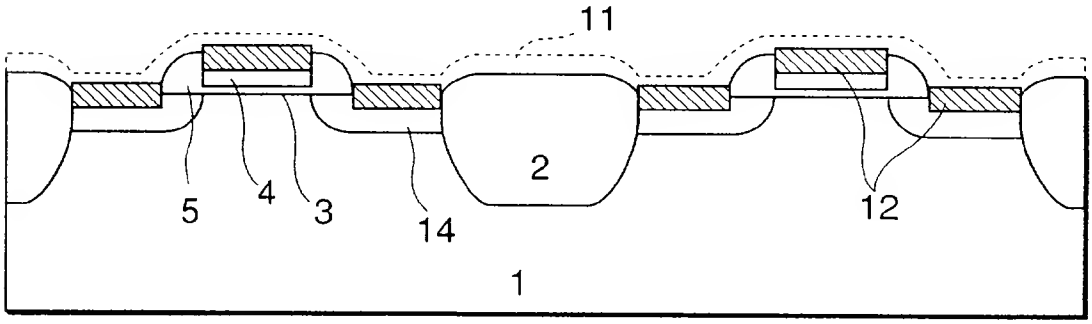


Fig.3(f)

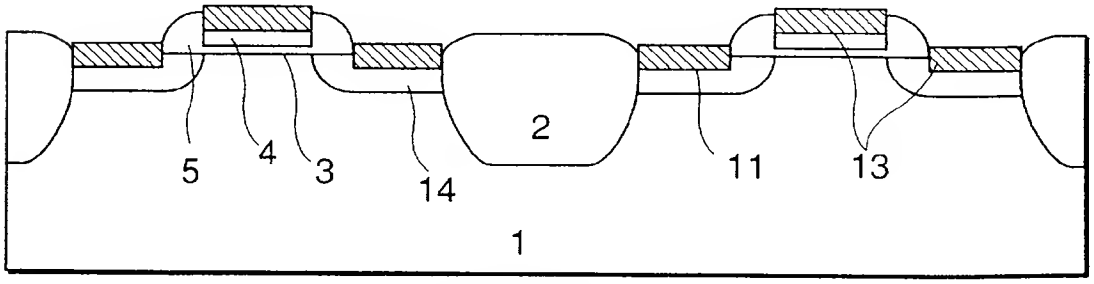


Fig.3(g)

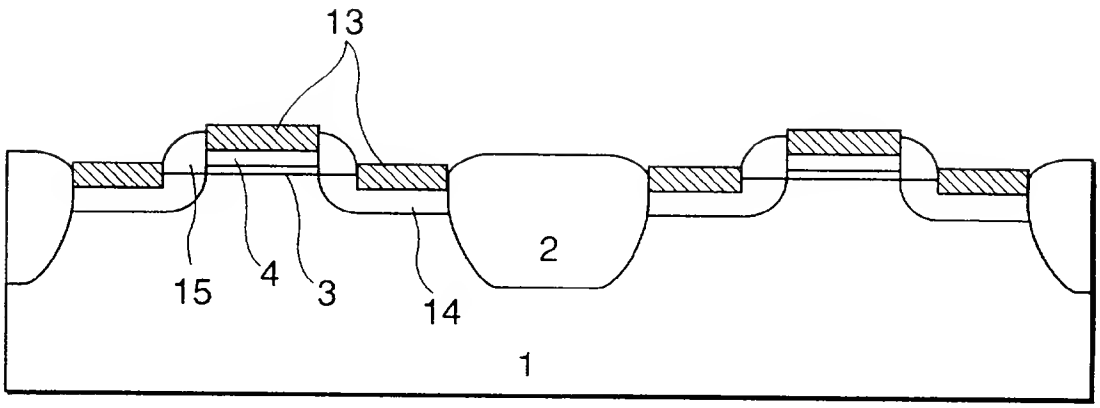
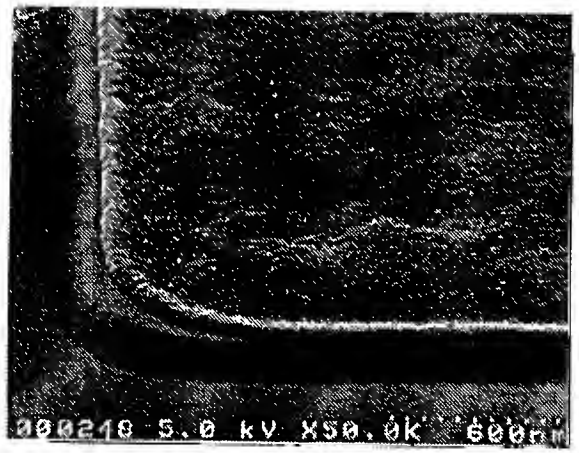
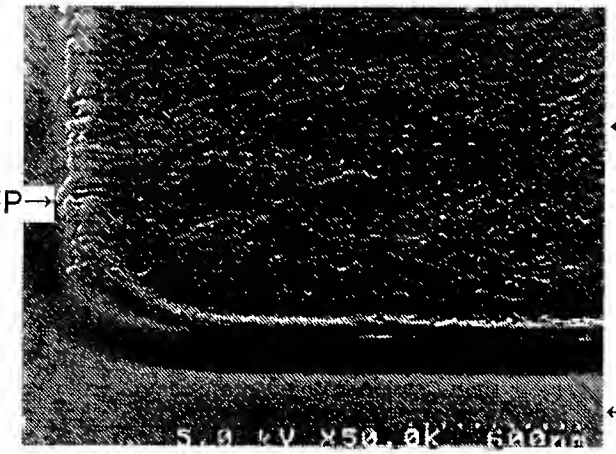


Fig.4



ION INJECTION:B^+

Fig.5(a)



ION INJECTION:BF^+

Fig.5(b)

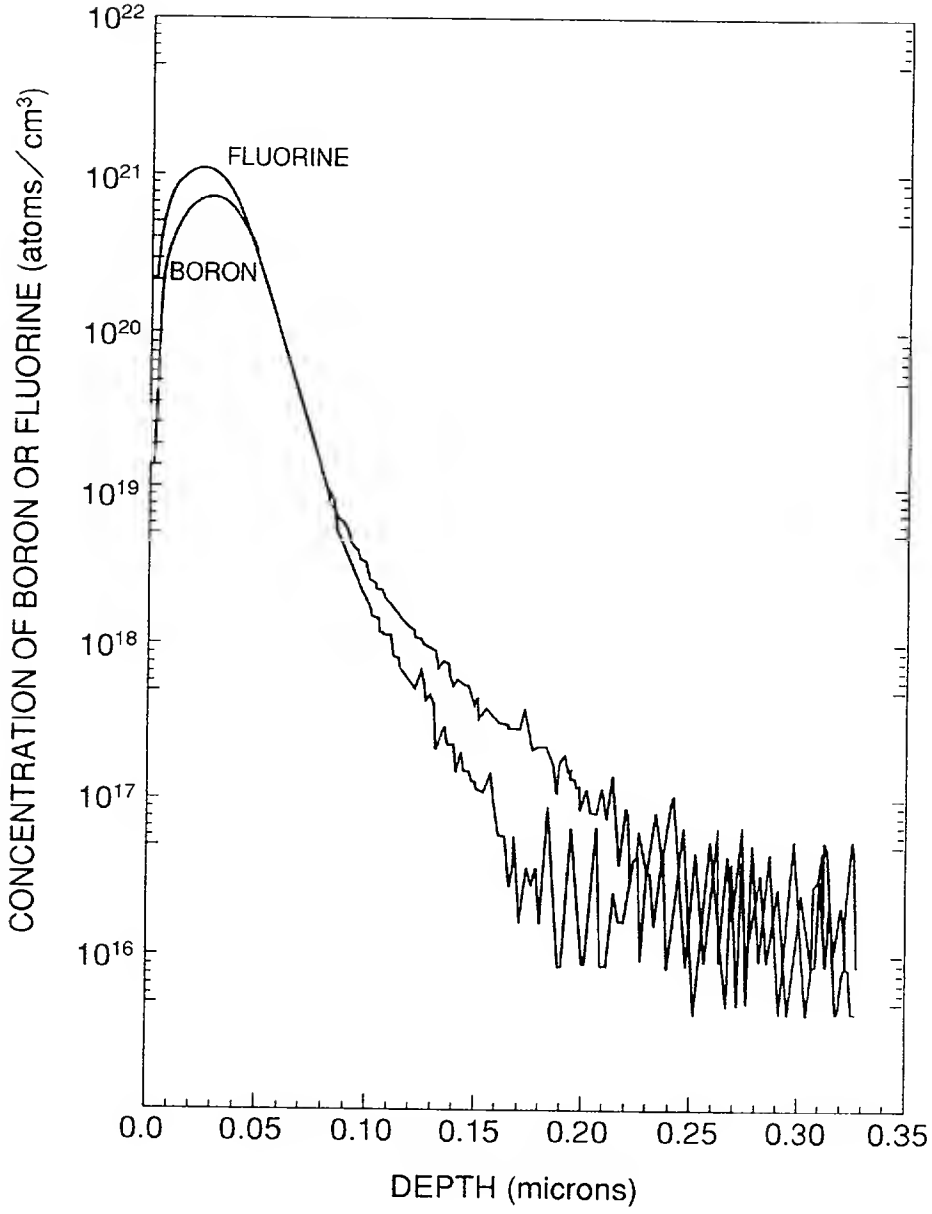
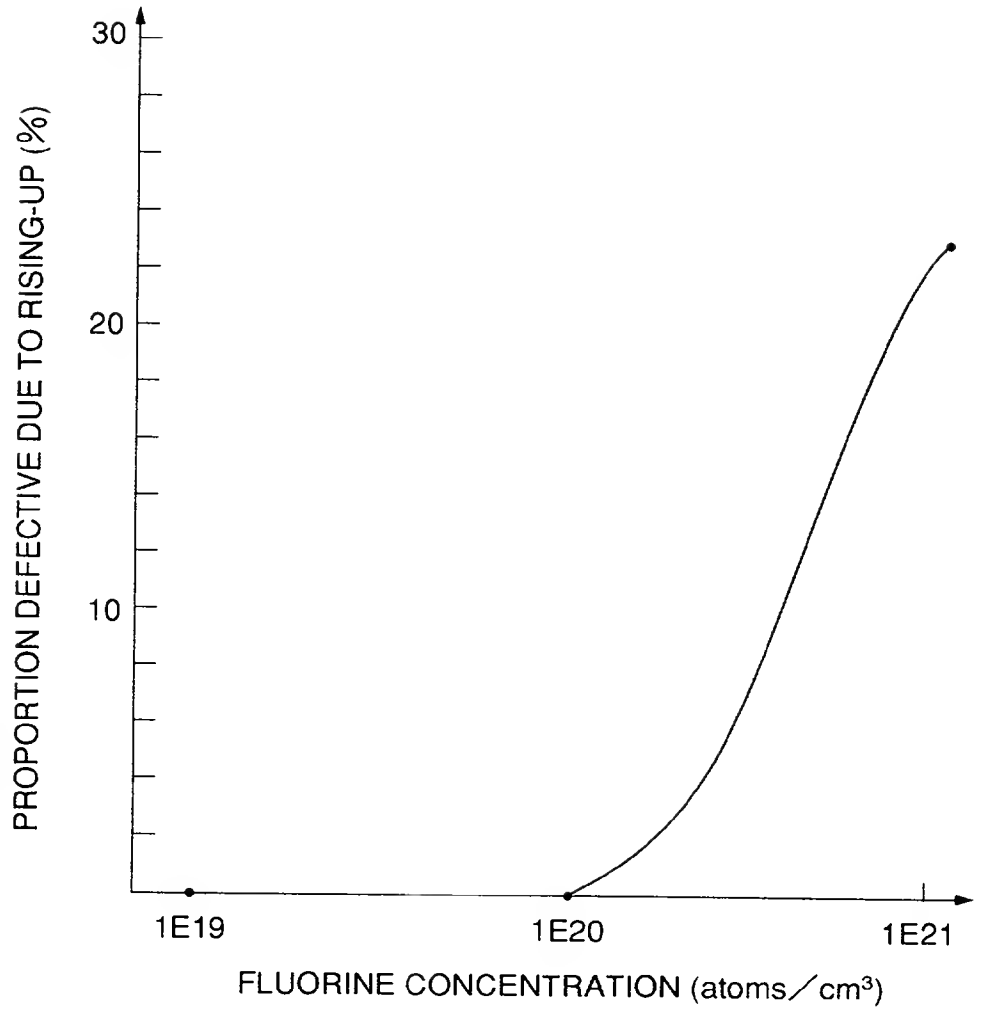

10^{22}
10^{21}
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
FLUORINE
BORON
CONCENTRATION OF BORON OR FLUORINE (atoms/cm³)
0.0
0.05
0.10
0.15
0.20
0.25
0.30
0.35
DEPTH (microns)

Fig.6



RELATION BETWEEN FLUORINE CONCENTRATION
AND PROPORTION DEFECTIVE DUE TO RISING-UP

Fig.7

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF FABRICATING SEMICONDUCTOR DEVICE FOR PREVENTING RISING-UP OF SILISIDE,
the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as

Application Serial No. _____

and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
149733/1997 (Number)	Japan (Country)	6/6/1997 (Day/Month/Year Filed)	☒ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

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Second Inventor's signature Date
Residence
Citizenship
Post Office Address

(Supply similar information and signature for third and subsequent joint inventors.)